Amendments to th Claims

This listing of claims will replace all prior versions, and listings, of claims in the application.

Claim 1. (original) An integrated circuit, comprising:

a semiconductor device;

a contact layer disposed outwardly from the semiconductor device and operable to provide electrical connection to the semiconductor device; and

a dielectric layer disposed inwardly from the contact layer and outwardly from the semiconductor device, the dielectric layer comprising an at least substantially porous dielectric material doped with at least one dopant.

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Claim 2. (original) The integrated circuit of Claim 1, wherein the dopant comprises at least one of phosphorus, fluorine, carbon, and boron.

Claim 3. (original) The integrated circuit of Claim 1, wherein the at least substantially porous dielectric material comprises an at least substantially porous oxide.

Claim 4. (original) The integrated circuit of Claim 1, wherein the semiconductor device comprises a transistor.

Claim 5. (original) The integrated circuit of Claim 1, further comprising a nitride layer disposed between at least a portion of the semiconductor device and the dielectric layer.

Claim 6. (original) A transistor, comprising:

a semiconductor substrate comprising a source region and a drain region;

a transistor gate disposed outwardly from the semiconductor substrate and between the source and drain regions;

a contact layer disposed outwardly from the semiconductor substrate and operable to provide electrical connection to the source and drain regions; and

a dielectric layer disposed inwardly from the contact layer and outwardly from the semiconductor substrate, the dielectric layer comprising an at least substantially porous dielectric material doped with at least one dopant.

Claim 7. (original) The transistor of Claim 6, wherein the dopant comprises at least one of phosphorus, fluorine, carbon, and boron.

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Claim 8. (original) The transistor of Claim 6, wherein the at least substantially porous dielectric material comprises an at least substantially porous oxide.

Claim 9. (original) The transistor of Claim 6, further comprising a gate dielectric disposed outwardly from the semiconductor substrate and inwardly from the transistor gate.

Claim 10. (original) The transistor of Claim 6, further comprising a nitride layer disposed between at least a portion of the semiconductor substrate and the dielectric layer.

Claims 11-20 (cancelled)

Claim 21. (currently amended) An integrated circuit, comprising:

a semiconductor substrate;

a lowermost metal interconnect layer formed over said semiconductor substrate;

a polysilicon/metal 1 dielectric (PMD) between said lowermost metal interconnect layer and the semiconductor substrate, the PMD comprising an at least substantially porous dielectric material doped with at least one dopant.

Claim 22. (previously presented) The integrated circuit of claim 21, wherein said at least one dopant comprises phosphorus.

C1 Claim 23. (previously presented)The integrated circuit of claim 21, wherein said at least one dopant comprises fluorine.

Claim 24. (previously presented)The integrated circuit of claim 21, wherein said at least one dopant comprises carbon.

Claim 25. (previously presented)The integrated circuit of claim 21, wherein said at least one dopant comprises boron.